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Real Time Signal Processing and Data Handling with dedicated hardware in handheld OCT Device

P. Guerra,[a,b,1] **J.J. Valverde,**[a] **A. Martin,**[c] **M.J. Ledesma,**[a,b] **J.L. Rubio-Guivernau**[c] **and A. Santos**[a,b]

[a] *Biomedical Image Technologies Universidad Politécnica de Madrid, ETS de Ingenieros de Telecomunicación, Ciudad Universitaria S/N, Madrid, Spain*
[b] *CIBER-BBN, Instituto de Salud Carlos III, C/ Monforte de Lemos 3-5 Pabelln 11 Planta 0, 28029 Madrid, Spain*
[c] *Medlumics SL, Ronda de Poniente, Tres Cantos, Spain*

E-mail: pedro.guerra@upm.es

ABSTRACT: The manuscript presents the topics on real time signal processing with dedicated hardware presented at the INFIERI Summer School 2014. The focus of this work is on real-time signal processing, filtering and massive parallel computing. In general, medical devices have stringed demands on energy consumption as well as on data processing and handling. In fact, the development of novel medical devices has led to significant advances in fields such as instrumentation, algorithm development and image processing.

In this manuscript, two aspects of the design are brought into consideration: the transformation of a conventional signal processing algorithm into an equivalent version that is suitable for hardware implementation and the use of on-chip modules originally developed for mass-electronics applications, for high speed data transmission. The development of a novel state-of-the-art handheld OCT probe is used to exemplify theses aspects. In particular, the "design process" behind the implementation of a multichannel quadrature coherent demodulator is disclosed.

KEYWORDS: Digital signal processing (DSP); Digital electronic circuits; Front-end electronics for detector readout

[1] Corresponding author.

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1 Introduction

Medical devices have to become more powerful, energy efficient, faster and smarter, with the goal of providing newer functionalities that help saving money and improving patient care. Current advances in medical imaging are made in fields such as instrumentation, diagnostics, and therapeutic applications and most of them are based on imaging technology and intensive image processing [1]. This applies to stationary and mobile medical devices alike, whether compact ultrasound devices, complex tomographic imaging devices, medical tablet, personal computers (PC) or patient data monitoring systems.

In many of these applications, it is required to acquire, process, move and display or store huge amounts of data in real time. At the same time, devices need to become more compact, energy efficient and cost effective in order to succeed in an increasingly mobile and wider field of application. Constraints are so demanding that usually dedicated electronic systems must be designed for the purpose. Several factors should be considered in the efficient development of flexible medical imaging instruments:

- Development of imaging algorithms involves multidisciplinary teams, with different backgrounds, who shall converge into an implementable solution. This requires high-level modelling tools for the analysis and evaluation of the proposed digital signal processing (DSP) algorithms.

- Real-time performance demands for system platforms, including hardware (HW) and software (SW), capable of satisfying strict time constraints. Finding the proper partitioning and task distribution between dedicated HW and SW requires a wide joint exploration of the design space [2].

- Current systems are capable of acquiring significant amounts of data that must be processed but also, in many situations, sent to a third party for further processing and/or storage.

In this manuscript, we review the process of transforming a signal processing algorithm with application in optical coherence tomography into an architecture that is suitable for hardware implementation. Then, we will briefly discuss the architectural elements of modern programmable devices that that allow high speed data streaming.

2 Optical Coherence Tomography

Optical Coherence Tomography (OCT) is a non-invasive imaging technique that falls in between ultrasound and microscopy. With an axial resolutions ranging from 1 to 15 μm, approximately and penetration depth in tissue around 1.5 mm, limited by light scattering, it is a technique that can be integrated with a wide range of instruments such as endoscopes, catheters, laparoscopes, or needles, which enable internal body imaging [3].

The velocity of propagation of light in biological tissues t is reduced from its speed in vacuum according to the index of refraction n of the medium. The functional form of the electric field E of a light wave is:

$$E_s(t) = E_s \cos\left(2\pi\nu t - \frac{2\pi}{\lambda} z\right) = E_s \cos(\omega t - kz) \tag{2.1}$$

Where υ is the wave frequency, ω is the angular frequency, k is the wavenumber and λ is the wavelength. These terms are coupled by the index of refraction.

OCT performs cross-sectional images (B-scans) of the tissue by measuring the magnitude and echo time of backscattered light along predefined lines (A-scan) using low-coherence interferometry, or white light interferometry. This technique performs correlation or interference between light backscattered by the tissue and light that has travelled though a reference arm. Hitherto, different versions of low-coherence interferometry have been developed for non-invasive measurement in biological tissues [4–7]. Figure 1 shows a schematic diagram of a simple Michelson interferometer in time domain. In this apparatus, the light propagates through two alternative paths, one through the reference arm with length l_r and other through the sample arm with length l_s. The field interfering at the detector generates a photocurrent proportional to the square sum of the fields, one backscattered from the sample E_S and other E_r which has been reflected by the mirror at the end of the reference arm at the detector.

Interferometry measures the field of the light rather than its intensity. The electric field at the output of the interferometer is the sum of the signal and reference fields, $E_r(t) + E_s(t)$, and a detec-

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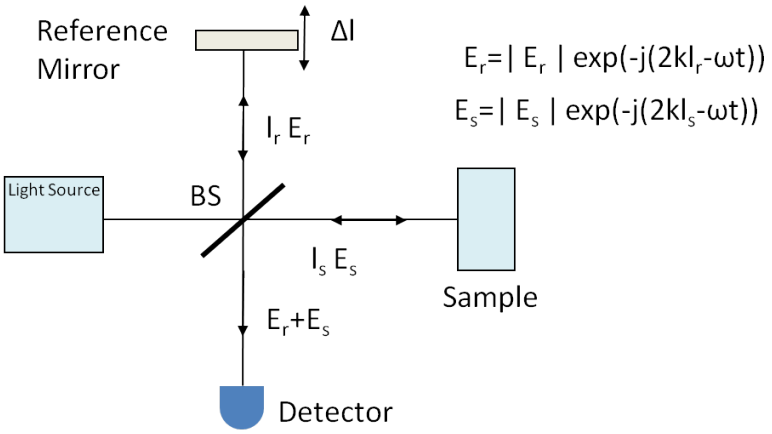

Figure 1. The Michelson interferometer. The reference mirrors and sample are positioned at distances l_r and l_s respectively from the beamsplitter (BS). If the light source is perfectly coherent (i.e., monochromatic), then reflection from the reference and sample mirrors produces a sum of two monochromatic electric field components, one backscattered from the sample E_S and other E_r which has been reflected by the mirror at the end of the reference arm at the detector.

tor measures the intensity I_o of the output, which is proportional to the square of the total field is:

$$I_o \sim |E_r|^2 + |E_s|^2 + 2|E_r||E_s| cos\left(\frac{2\pi}{\lambda/2}\Delta L\right)$$
$$I_o \sim DC + 2|E_r|E_s| cos\left(\frac{2v_s}{v_m}\omega\Delta t\right) \tag{2.2}$$

Where, λ is the laser's wavelength, v_m is the speed of light in the medium, v_s is the speed at which the mirror is moving, ΔL is the path length difference between the signal and reference arms of the interferometer. The continous term (DC) depends on the amplitude of the reference and backscattered beams and the cross term, describes the variation of the photocurrent with the positions of the reference and sample mirrors. This equation shows that the sinusoidally varying term in photocurrent represents the interference between the reference and sample fields and contains all of the information related to the sample.

The intensity provides information about the tissue microstructure, but it is also possible to extract information about movements, which is the case of blood flow. This functional extension of OCT has become variously known as optical Doppler tomography, colour Doppler OCT, or Doppler OCT (D-OCT) [8]. There are several approaches for detecting tissue blood flow using OCT [9, 10]. One viable approach for OCT Doppler flow imaging is to detect the local phase changes by comparing adjacent A-scans [11–13]. A widely used velocity estimation method in Doppler ultrasound for real-time flow imaging is based on calculating the phase change between successive echoes from moving blood [14]. In time-domain D-OCT, this is implemented by performing a quadrature demodulation of the interferometric signal and estimating the phase information with the Kasai algorithm.

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3 Architecture of a Hand-held OCT probe

The system under consideration aims at the development of a cost effective, reliable and compact optical biopsy tool for dermatology and point-of-care diagnosis. The system includes a pen-like OCT probe and an associate console on which the acquired images are to be displayed and analyzed. In this probe, the splitter and the reference arms have been implemented using integrated optics, while the external source and detectors are currently coupled with optical fibers. Thanks to the integration, the varying group delay in the reference arm of the Michelson interferometer is obtained by means of the thermo-optic effect of silicon [15]. This approach reduces the complexity, footprint and accurate mechanical adjustments needed in conventional time-domain OCT implementations [16], which resort to a tilting mirror and a grating to implement the delay line.

In our particular implementation of the delay line [17], a plurality of waveguides are integrated on the substrate to combine the reference light with the backscattered light and thus resolve contributions from a plurality of points at the sample [18]. The retrieval of the OCT information requires simultaneously demodulating the different contributions to reconstruct the sample information. Currently, the integrated optics device enables the concurrent exploration of four different channels. The proposed architecture for OCT data retrieval, shown in figure 2, includes one analog to digital converter (ADC), four quadrature channels to demodulate the coherent signal and build the A-Scan line. Images are streamed to an external platform by a hardware implementation of the User Datagram Protocol (UDP), which is part of the internet protocol (IP) stack.

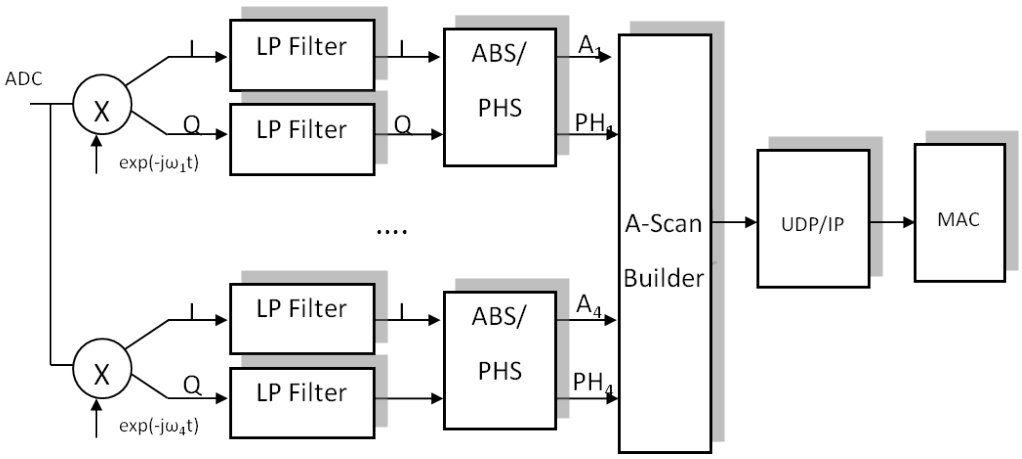

Figure 2. Proposed architecture for OCT data retrieval. Different channels are demodulated to build the A-Scan line. Images are streamed by a hardware implementation of the UDP/UP protocol.

Signal demodulation is achieved by direct down conversion of the OCT signal sections, taking into account the central frequency ω_i of the OCT signal, low-pass (LP) filtering of the inphase (I) and quadrature (Q) components to reject adjacent information and finally computing the amplitude (ABS) and phase (PHS) of the I/Q signals. Moreover, the high amount of data being acquired and the unidirectional direction of the flow justify the development of hardware accelerated implementation of the UDP/IP protocol stack [19–21]. This HW-based processing module is able to sustain high data rates, above 800 Mbps, while keeping the overall system complexity moderate, avoiding the need of an additional microprocessor.

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4 Implementation of the digital quadrature demodulation

The Digital signal processing (DSP) algorithms used to demodulate and build the OCT image are typically specified as infinite precision operations. On the other hand, their actual implementation on a field programmable gate array (FPGA) relies on fixed-point approximations. One essential step of a top-down design flow is to determine the numerical accuracy at every signal node, namely the word-length, truncation mode and overflow mode, need to fulfil the constraints of the application. This is commonly referred as floating-point to fixed-point conversion (FFC) problem. Conventional approaches are typically both time-consuming and error-prone since ad-hoc assignments of fixed-point data type are performed manually and iteratively [22].

In the process of implementing a given algorithm into HW following a top-down design flow, we usually face two well defined stages, that of transforming the ideal algorithm into a functionally equivalent version that is efficient of HW implementation, i.e. that only uses integer values to represent numbers, and that of determining the architecture, to maximize parallelism [23].

4.1 Floating to fixed point conversion rules

In the case of dedicated electronics, implemented with Application Specific Integrated Circuits (ASICs) or FPGAs, the implementation of a given algorithm with integer fixed-point arithmetic enables the implementation of highly parallel processing pipelines capable of massive data processing. In order to represent a real number with fixed point, the number of fractional bits n and integer bits m has to be specified. This results in the well known Q-notation where the integer value X with representation $Q(m_1,n_1)$ is used to represent the real number $Z = X * 2^{-n1}$, being the total word length $wl = n_1 + m_1 + 1$, where X is an integer represented in two's complement.

> *Example*:
>
> The $Q(4,4)$ Fixed-point representation of 2.875 is $46 * 2^{-4}$, which in binary form is equivalent to 00010.1110.
>
> In $Q(4,4)$ the dynamic rages is $[-256,255] * 2^{-4}$

From a practical point of view, we have to point out that when implementing a signal processing algorithm in fixed point the $Q(m_1,n_1)$ representation is implicit, in the sense that the number of bits devoted to represent the fractional and integer part part of a given variable are not automatically supported by the tool, be it a compiler or a logic synthesis tool, and it is the designer who must properly track the number representation after each operation and usually needs to explain bit manipulations in his code as side comments. That implies that, in order to perform arithmetic computations with numbers in fixed-point certain rules, summarized in the following table, have to be taken into account manually to properly track the evolution of the fixed point representation after each operation.

The transformation of any algorithm into fixed-point requires specifying the dynamic range and needed numerical accuracy for every variable and intermediate result in the algorithm, which is a time consuming task. Hence, different methodologies have been proposed to automatically determine word lengths and thus quickly explore alternative architectures and implementations [24–26]. To exemplify the fixed point conversion process, this manuscript details the development of an infinite impulse response (IIR) filter from specification to implementation.

Table 1. Fundamental Rules for Fixed-point manipulation.

Input Representation	Output Representation	Observation
$Q(m1,n1)+Q(m1,n1)$	$Q(m1+1,n1)$	Fractional bits shall be equal
$Q(m1,n1)*Q(m2,n2)$	$Q(m1+m2+1,n1+n2)$	Multiplications cause a significant growth in word length, periodically the word has to be resized an some bits discarded
$Q(m1,n1)/Q(m2,n2)$	$Q(m1+n2+1,n1-n2)$	Division is an expensive operation in hardware
Sum$(Q(m1,n1),i$ times$)$	$Q(m1+log2(i),n1)$	Case of vector or matrix multiplications
Sqrt$(Q(m1,n1))$	$Q($upper$(m1/2),n1/2)$	Fractional bits shall be even

4.2 Quadrature Receiver Implementation

As it is shown in table 1, the mixer is implemented as two tables, to store sine and cosine values, which are indexed using the phase value and a pair of multipliers. The phase value is incremented every clock cycle by a fixed amount to generate the oscillating signal with the desired frequency.

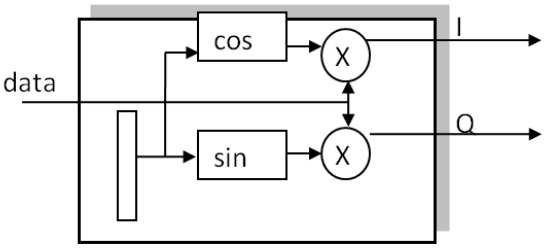

Figure 3. Block diagram for the quadrature mixer.

Multiple alternatives are possible to the implementation of a narrowband low pass or band pass filter. However, the filter order needed to achieve high frequency selectivity with a finite impulse response (FIR) approach is so high that other architectures, such as cascaded integrator-com (CIC) [27] filters or infinite impulse response (IIR) are chose to provides a reasonable resource/performance trade-off. For a given frequency response it is well known that IIR filters can do with much less hardware resources than Fir filters but at the expense of a nonlinear phase response. An IIR filter consists of a transfer function $H(z)$ with q poles and p zeros. In the literature, multiple variations are described. These include among others, the following:

- Direct form I and direct form II, transposed or not.
- Lattice-ladder canonical forms [28].
- Wave digital filter [29, 30].

These alternative implementations are ideally equivalent but this is not the case when taking into account the non-linear effects introduced by fixed point quantization. Particularly, the frequency response can be very sensitive to variations in coefficient values. Small changes due to quantization may cause a significant displacement in the roots of the H(z) function, and may even cause the filter to become unstable. The direct form I is often used by fixed-point IIR filters since a larger single adder can be used to prevent saturation. By comparison, direct form II is often used

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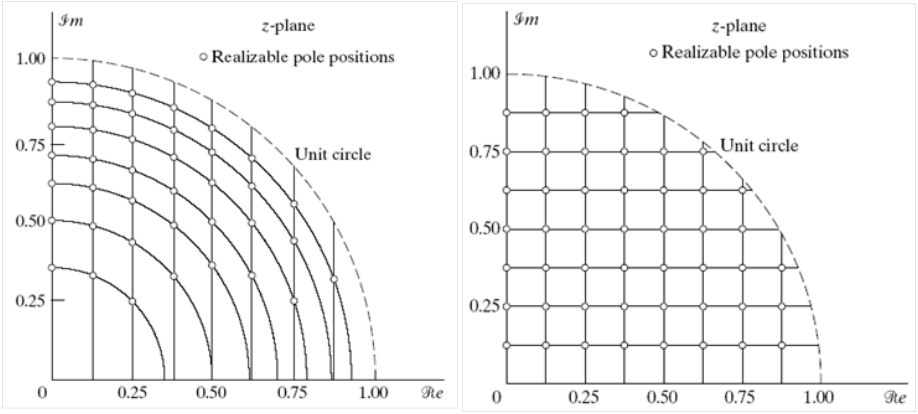

Figure 4. Possible pole locations for three-magnitude-bit coefficient quantization in the standard direct I second order section (left) and coupled –form order (right).

by floating-point IIR filters, since it uses fewer states and the adders are not as sensitive to saturation. In fact, Jackson et al. [31] showed that second-order sections (SOS) optimized in isolation and connected in cascade, called sectional optimal structures, perform very close to block optimal cascades. However, as its shown in figure 1, the location of realizable poles places some limits on the realization of narrowband low-pass fixed-point filtering with direct form I architectures. Fortunately it is well known that coupled-form second order IIR filters, also called the Gold-Rader filter [32], enable second-order narrowband low-pass IIR filters with poles, at the cost or doubling the number of multipliers needed.

In a SOS fixed-point implementation, whose architecture is represented in figure 5, there are many possible pole-zero pairings and section ordering, which are arithmetically equivalent but produce very different quantized outputs. As a rule of thumb, pole/zeroes should be chosen to be as close to each other as possible, so that their net effect partially cancel and thus minimize the frequency response changes at the output of each section [33]. Any given SOS section, has a complex conjugate pole pair $z_p = r_p \exp(\pm j\theta_p)$ in the negative real region and two effective zeros $z_z = r_z \exp(\pm j\theta_z)$. This is summarizes as:

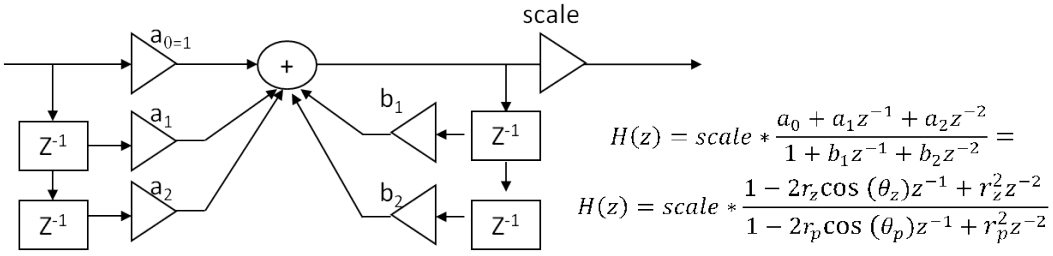

Figure 5. Block diagram of direct form I second-order IIR structure. It may be concluded that filter coefficients are bounded, that is $-2 \leq (a_i, b_i) \leq 2$.

4.3 Quadrature Receiver: fixed point conversion

The ultimate goal is to implement a parameterizable HDL block for IIR low pass filtering, which may be automatically generated with a high level tool, such as Matlab (The Mathworks, Natick, MA, U.S.A.) and synthesized into an FPGA. After considering alternative architectures, it is decided to implement the IIR structure as a cascade of biquadratic or second-order sections (SOS). The biquad implementation is particularly useful for fixed point implementations, as the effects of quantization and numerical stability are of no great concern. However, the overall success of any biquad implementation is dependent upon the available number precision, which must be sufficient enough in order to ensure that the quantized poles are always inside the unit circle.

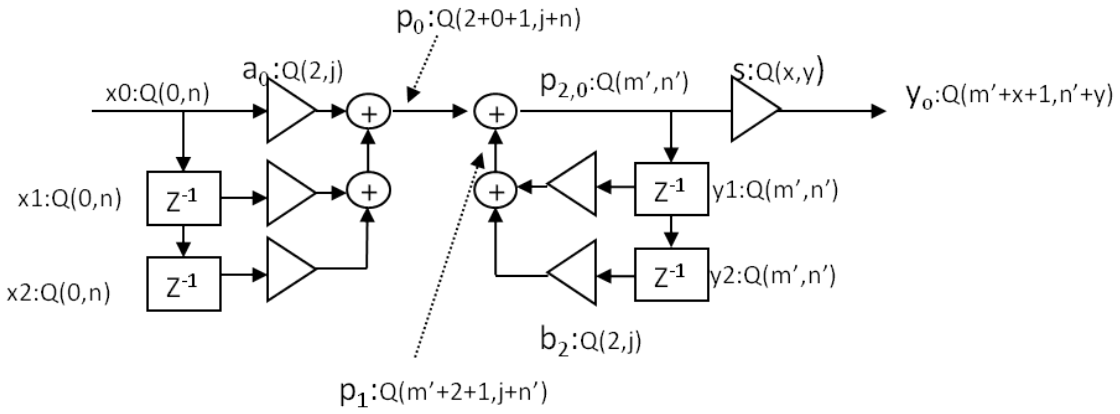

Figure 6. Fixed point analysis of the module. For the sake of clarity, we will assume that the scale factor and the representation after scaling is the same for all SOS modules. In our case, we have to specify the representation of the biquad output y_i, the internal representation $p_{2,i}$ as well as that of the scaling s and filter coefficients.

In figure 2 we summarize the optimization analysis of an 8th-order Butterworth low-pass filter implementation with $Wn = 0.1$. To evaluate the approximation goodness, the max relative error between the floating point implementation and fixed point implementation are compared at different points of the algorithm. The following plot shows the evolution of the error when sweeping the number of fractional bits of one variable and keeping the rest at the maximum (i.e. 24 bits). The first plot (upper-left), sweeps along the fractional accuracy of the biquad output variable (y_o); the second plot explores the required accuracy to represent the output scale factor (S), the third plot explores the quantization error due to the representation of the internal biquad variables ($p_{2,0}$); last but not least, the four plot explores the requirements on the number of fraction bits needed for the filter coefficients (a_i and b_i). It is observed that the limiting factors in this error are the accuracy in the filter and scale factors. This is most likely due to the limitations imposed by a direct form I architecture in the implementation of a narrowband low-pass filter.

Once the accuracy representation is determined, the analysis of the dynamic range at internal nodes helps us finding the number of integer bits that are required. In this case, figure 3 shows the evolution of the SOS outputs at $p_{2,i}$ and y_i filter, and proves that the selected representation after the analysis, summarized in table 1, is correct.

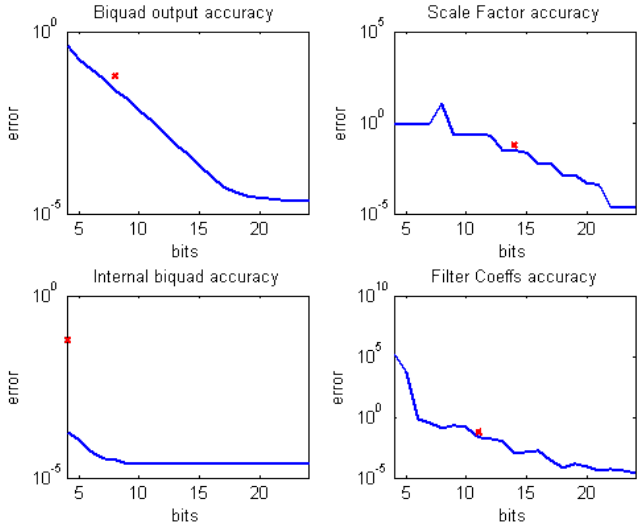

Figure 7. Error with respect to the impulse response computed with full precision and with fixed-point representation.

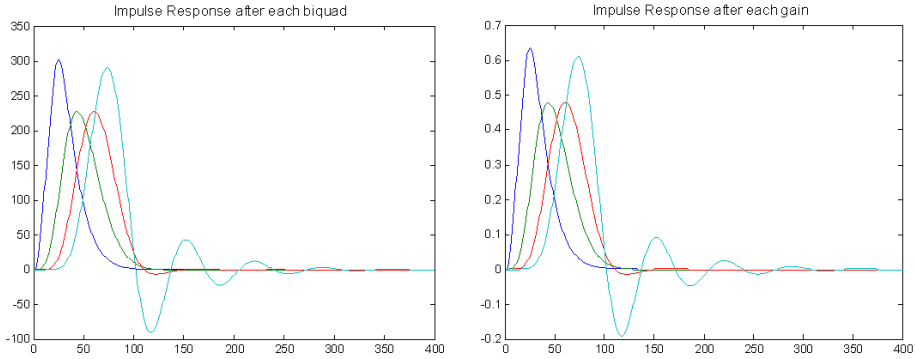

Figure 8. Fixed-point impulse response at $p_{2,i}$ and y_i.

After these simulations, we have constrained our internal representations to the values summarized in the following table.

Table 2. Final data representation

Articolo I. Node Name	Articolo II. Fixed Point Requirements
x0	Q(0,12)
a_i	Q(2,11)
b_j	Q(2,11)
p_0	Q(3,23)
p_1	Q(12,15)
p_2	Q(9,4)
y0	Q(0,8)

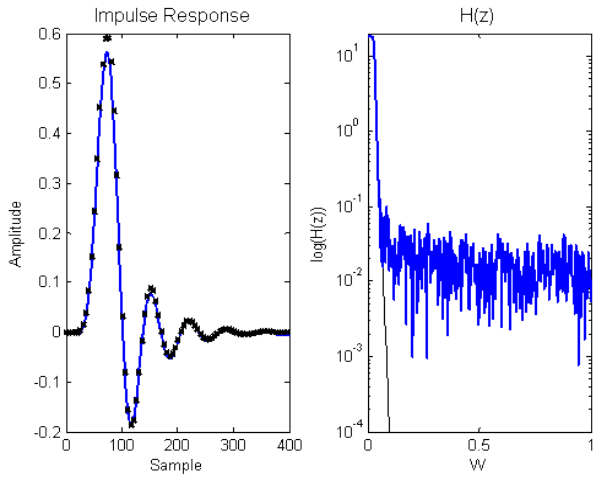

Figure 9. Floating point impulse response (black) vs fixed point counterpart (blue) in time (Left) and frequency (Right) domain in log-scale.

With these representations, the partial time response after each SOS, shown in figure 8, shows no clear distortion due to quantization, and the global time and frequency responses, shown in figure 9, show that the final fixed-point implementation is very close to that of the ideal one.

4.4 Quadrature Receiver: algorithm Pipeline

The pipelining of the SOS module, show in figure 10, is straightforward: registers are inserted at regular points as shown in the following figure, which does not show fixed-point word length adjustment blocks. These intermediate registers increase the algorithm latency, reduce the combinational complexity between registers without affecting the numerical result and eases the automatic generation of high order filters as a cascade of this building block. According to synthesis results with an Artix-7 FPGA (Xilinx, Logic Drive, San Jose CA, U.S.A.), this architecture would support data processing with sampling rates up to 90 MHz and independent of the filter order.

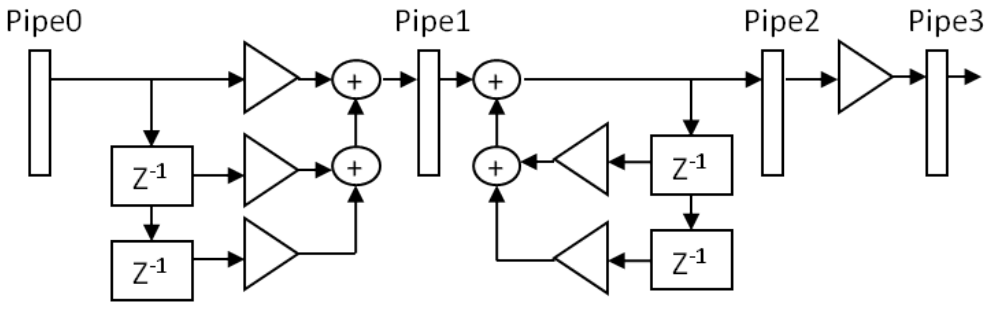

Figure 10. Block diagram of the pipelined biquad structure that is used as building block of the filter 8th order IIR low-pass filter used to select the OCT channel of interest.

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4.5 Implementation of a UDP/IP HW module for high speed data streaming

In this context, a dedicated module has been implemented to send a continuous data flow over an Ethernet network using off-the-shelf components. Data is encapsulated as UDP datagrams [34], which are built by a hardware module in the FPGA and sent to user configurable destination ports.

This communication module connects to an on-chip medium access controller [35], that handles the interface with an external gigabit transceiver (88E1111, Marvell, Hamilton Bermuda). Additional connectivity to a microprocessor (uP) is provided to enable bidirectional communication with the acquisition system via software. Moreover, a light weight custom implementation of the ARP level is used by the module to determine the MAC address of the destination.

Input data, organized as lines, are buffered in a first-first out (FIFO) buffer. Whenever a full line is waiting for transmission, a finite state machine builds the datagram, including cyclic redundancy checks, transfers it to a second FIFO and request the MAC to start the transmission and sends data to the external gigabit transceiver. It has been measured that the module transfers the input data without any loss up to 800 Mbit/s.

5 Results

The implemented architecture is configured for four OCT demodulation channels, with central frequencies at 1.5, 1.7, 2.0, 2.3 MHz, spectral bandwidths of 90 KHz and a sampling rate of 12.5MHz. Low pass filters are designed to guarantee adjacent-channel rejection higher than 100 dB. The dimensioning the word sizes is carried out with this constraint in mind. As an example, figure 11 shows the generation of the A-scan for the forth reception channel, including the evolution of the digital signals at different stages of the demodulation process.

In the previous diagram the demodulator steps needed to produce A-scan line are shown. The information from each channel, properly multiplexed and synchronized in time with the exploration control signals, enable the composition of a B-scan image, as shown in figure 12. Currently, the system is configured for the generation of 850 lines per second, yielding 1 B-scan image per second, with size 850x512 pixels.

6 Conclusions

Fuelled by the development of an innovative technology for integrated optics, the design of a portable time-domain optical coherence tomography (OCT) probe has been made possible. As part of this compact OCT system, a module for multi-channel coherent demodulation of the interferometric signals has been specified and implemented.

Significant effort has been needed in the front-end processing to meet the demanding design constraints in terms of noise rejection, numerical accuracy and band selectivity. The benefits and limitations of very narrow low-pass IIR filters have been widely described in the literature, and alternative architectures have been considered during this work. The processing hardware core has been highly parameterized, so that the complete module can be automatically generated with the aid of a scripting tool. Currently, the probe already produces high quality images of the skin. However future generations of the integrated optical device will demand for even sharper filters that

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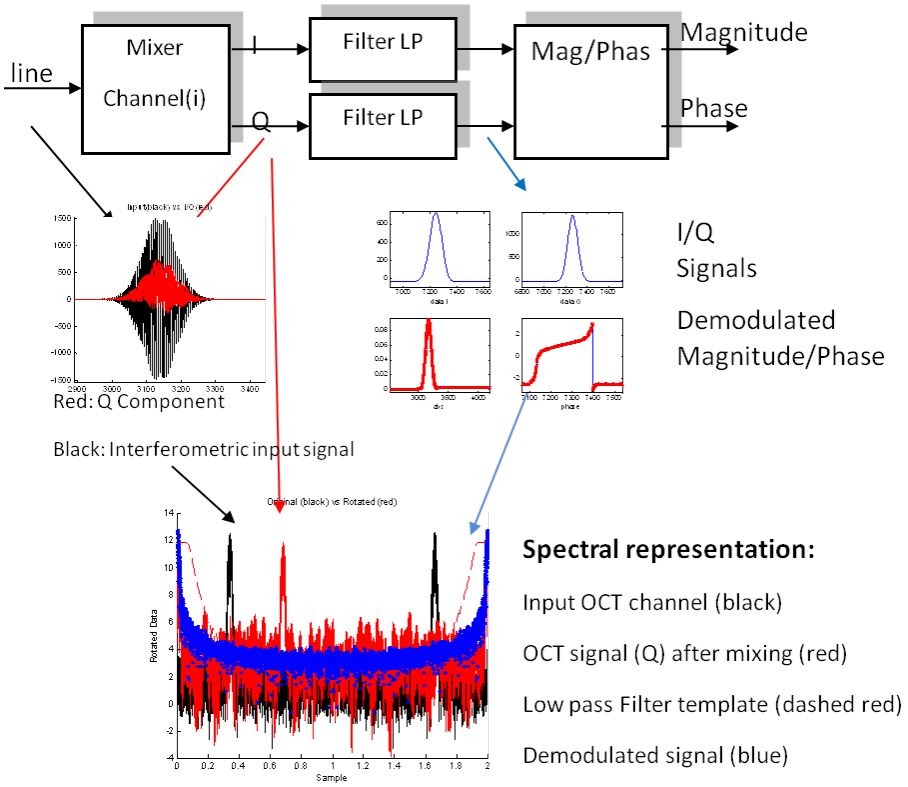

Figure 11. Diagram showing the generation of the A-scan for the 4^{th} reception channel. These data are obtained simulating the behavior of synthesizable description of the hardware that is to be implemented in the FPGA.

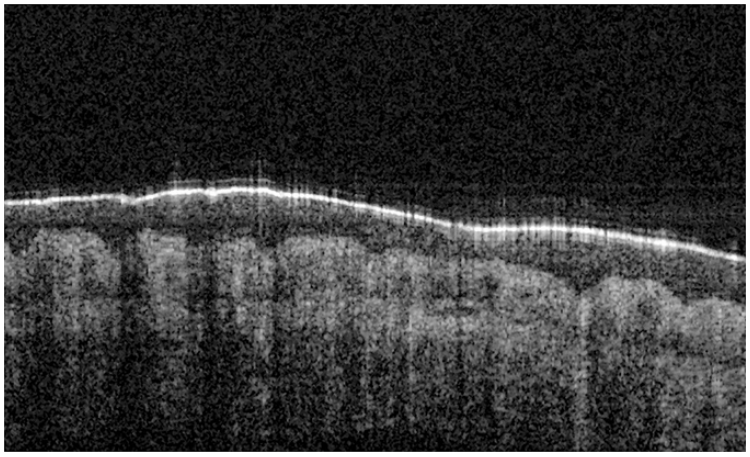

Figure 12. B-scan raw OCT image of the skin, resulting from the direct composition of A-scan lines without further post-processing.

may require new processing architectures. In this line, multirate techniques may provide a viable approach to further narrow the pass band without compromising filter stability.

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