

Tools for Electronic Design

Course Description

Pablo Ituero Herrero



Departamento de
Ingeniería
Electrónica

Universidad Politécnica de Madrid

Máster Oficial en Ingeniería
de Sistemas Electrónicos

www.die.upm.es



Index

Tools for Electronic Design.....	2
Objectives.....	2
Program.....	3
Bibliography	3
Teachers	4
Teaching Methodology	4
Evaluation.....	4
Contact	4

Tools for Electronic Design

Semester: 2

Number of credits: 4 (2 practical and 2 theory)

Type: Optional

Objectives

This course aims to train students in the use of CAD tools for digital integrated circuit design, with special attention to the phases of synthesis, simulation, physical design and verification. On each topic will be a series of labs with professional tools and methodologies used in the electronics industry based on workflow standard cells.

Specific objectives:

- The student will understand and assess general combinatorial optimization methods that use CAD tools.
- The student will be familiar with the parameters that describe a standard cell library.
- The student will understand the algorithms involved in logic synthesis and technology equivalence of combinational and sequential circuits, and high-level synthesis. The student will be able to synthesize a circuit described in VHDL language using the tool "Synopsys Design Compiler" and characterize the synthesized circuit. The student will become familiar with the types of files provided by manufacturers of standard cells for synthesis.
- The student will understand the algorithms involved in various types of electronic circuit simulation. The student will be able to perform pre-synthesis simulations, post-

synthesis and post-place & route using the tool "Modelsim". The student will become familiar with the types of delay models provided by manufacturers of standard cells for synthesis.

- The student will understand the algorithms involved in VLSI physical design phase: floorplanning, placement, routing and special routed. The student will be able to perform the physical design of a circuit synthesized using the tool "Cadence SOC Encounter", performing electrical and physical verification and characterization. The student will become familiar with the types of files provided by manufacturers of standard cells for physical design.
- The student will understand the most common techniques for the verification of digital circuits. The student will become familiar with SystemVerilog and verification methodologies oriented at UVM 1.1. Students will be able to verify a circuit described in VHDL following the guidelines described by UVM 1.1.

Program

The course consists of lectures and a series of associated practices will develop in pairs in the laboratory of Building B (B-043). Each pair is assigned a duty to choose between morning or afternoon. Each shift is three hours. Agenda:

- Introduction (0.5 ECTS). Design methodologies. Standard cell libraries. Methods for general purpose combinatorial optimization. Laboratory: Analysis of a standard cell library.
- Synthesis (0.75 ECTS). Optimization and synthesis of combinational logic. Optimization of two-level logic. Optimization of multi-level logic. Sequential Logic Design: FSM synthesis. High-level synthesis. Task planning and allocation. Algorithms in CAD tools. Synthesis on FPGAs. Laboratory: Synthesis and characterization with Synopsys.
- Simulation (0.75 ECTS). Simulation types. Cell models. Delay Models. Formal Verification. Static timing analysis. Transistor-level simulation. Laboratory: Simulation with Modelsim.
- Physical Design (1 ECTS). Partition. Placing objects on 0-d. Placing objects in 1-d. Placing objects in 2-D. Global Connection. Channel Connection. Detailed Connection. Clock and Power Piping. Laboratory: Physical Design with Cadence SoC Encounter.
- Verification (1 ECTS). Introduction to verification. System level verification. Functional coverage. Statements (assertions). Introduction to SystemVerilog. UVM 1.1. Laboratory: system level verification with SystemVerilog UVM along the lines of 1.1.

Bibliography

- Notes subject practices.
- Integrated Circuit Application-Specific. Michael John Sebastian Smith. Addison-Wesley. 1997.

- Algorithms for VLSI Physical Design Automation. Naveed Sherwani. KAP. 1999. Third Edition.
- Algorithms for VLSI Design Automation. Sabih H. Gerez. Wiley. 1998.
- Digital VLSI Chip Design with Cadence and Synopsys CAD Tools. Erik Brunvand. Addison-Wesley. 2010.
- SystemVerilog for Verification: A Guide to Learning the Testbench Language Features. Chris Spear. 2012.

In general these references must add manuals used CAD tools and publications of the scientific literature related to end practice.

Teachers

Coordinator: Pablo Ituero Herrero.

Teachers:

- Carlos Carreras Vaquer
- Marisa López Vallejo
- Ruzica Jevtic
- Pablo Ituero Herrero

Teaching Methodology

The course is proposed as a mixture of lectures, which give a theoretical on algorithms and methodologies, plus a laboratory session where they put into practice the concepts learned. At the end of the internship students will submit a report to justify the work performed and results obtained. For each subject, the teacher will select two practice teams that will have to do a presentation with the results and participate in a discussion about their design decisions.

Evaluation

Partial multiple choice of items 1, 2 and 3. 25%

Partial multiple choice of items 4 and 5. 25%

Technical quality of the practices. 40%

Class participation and technical skills demonstrated in the laboratory sessions. 10%

Contact

Pablo Ituero: pituero@die.upm.es

Desk: C-226

