# Microelectrónics (MCRE 1)

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# Index

Objectives	. 2
Program	. 3
Bibliography	
Teachers	. 4
Teaching Methodology	. 4
Evaluation	. 5
Contact	. 5

# **Microelectrónics (MCRE 1)**

#### Semester: 1

Number of credits: 4,5 (2,5 theory + 2 practical)

#### Type: optional

#### **Objectives**

The subject "Microelectronics" aims to train students of the Master in full-custom design of VLSI integrated circuits. This course provides a bridge between design and technology systems, processes and devices, considering the requirements of the circuits and systems that make use of these technologies.

This course aims to provide future designers vision systems covering hardware from system design aspects to the physical path, through their circuits and building blocks, mainly focused on CMOS technology, which is the most used today for circuit design application. It will also ensure a basic introduction to the structures and processes in the work necessary technology integrated circuit design.

Detailed objectives of the course are:

1. Achieve a thorough knowledge of the operation of MOS transistors.

2. Knowing the basics of the manufacturing process and the implications for the designer: the design rules.

3. Being able to design from schematic to layout any CMOS circuit.

4. Studying how to characterize CMOS designs in its main aspects: area, strength, capacity and delay.

5. Perform the design of CMOS logic gates following different architectures.

6. Design and analyze basic sequential circuits (t latch register)

7. Knowing different timing systems integrated circuits and associated implications.

8. Design subsystems (finite state machines, memories, data paths).

9. Learn VLSI design methods: since the completion of the base plane to complete the validation circuit.

10. Learn the basic principles of manufacturing test and how to take into account in the design.

#### Program

Introduction to the design of ASICs (0.3 ECTS)
 VLSI Design
 CAD Tools
 Representation of circuits and systems

2. NMOS and CMOS Logic: Bar Charts Switch logic

Transistors: operation
 investors
 Logic gates

4. Basic CMOS manufacturing processes. Design RulesSilicon semiconductor technologyBasic CMOS ProcessDesign Rules

5. Circuit characterization
resistance
capacity
Switching characteristics. retardation
Excitation of large capacity
Power consumption (static and dynamic). Dimensioning of power tracks;
"Latchup"

6. Sequential Logic Timing system Records Stack (FIFO)

7. Timing Strict two-phase approach Extensions to the basic timing



3

Generating a clock signal Timing alternatives Timed CMOS logic structures;

8. Subsystems design (1): PLA, Finite State Machine

9. Subsystems design (2): Adders, shifters Memory: RAM, ROM

CMOS design methods
 Input / output chip
 Structured Design Base Plan
 Alternatives CMOS chip design (Networks predifundidas, standard cell library, full-custom, FPGAs, ...)

11. Test of Integrated Circuits. Design for test Need test Controllability, Observability and Fault Models Design Strategies for test: Techniques "ad-hoc" structured techniques Techniques for self-test System Level Test

#### **Bibliography**

**N. Weste, D. Harris** (Libro de referencia). *CMOS VLSI Design: A Circuits and Systems Perspective* Pearson Addison Wesley, 2005

J.M. Rabaey Digital Integrated Circuits: A Design Perspective Prentice Hall, 1996

**N. Weste, K. Eshraghian** *Principles of CMOS VLSI Design: A Systems Perspective* Addison Wesley, 1993.

#### **Teachers**

Coordinator: Marisa López Vallejo.

Teachers: Marisa López Vallejo.

Pablo Ituero Herrero

# **Teaching Methodology**

The course is given in person, by combining the following methodologies:

- Lectures on theoretical and practical part. They will be in the classroom using transparencies and blackboard. At least 25% of classes are practical.
- Individual Exercises, delivered and corrected in class.
- Realization of a group project.

### **Evaluation**

The evaluation of the course is done through three sources:

- A written examination (40%). In it the student, with or without the use of reference books or notes as appropriate, must solve problems, designs or aspects based questions developed in class.

- Delivery of practical work and exercises (50%).

- Participation in class (10%).

# Contact

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- www.lsi.die.upm.es/~marisa/mcre.html
- http://moodle.upm.es/titulaciones/oficiales/course/view.php?id=2577

