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Descriptives 1.Datos

DIGITAL ELECTRONICS

Tutorial - Student Information

Subject

Digital Electronics

Matter

M5. Electronics

Department responsible

Electronic Engineering

ECTS credits

3

Character

Compulsory

Degree

Diploma in Engineering Technology and Services Telecommunication

Course

2 °

Specialty

N / A

Academic year

2012-2013

Semester in which imparts

First

Language in which imparts

Castilian

Website

http://moodle.upm.es/titulaciones/oficiales

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DESCRIPTION OF THE COURSE

The main objective of this course is to obtain a basic level of Digital Electronics knowledge and set the stage to perform the analysis and design of complex digital electronic circuits. This training is subjects completed in subsequent courses such as: Circuits Electronics, Digital Systems I and II, Electronic Systems Engineering, Processor Architecture and Design of Digital Electronic Systems.

The most significant evolution of digital electronics in recent years has been on the degree of complexity of the systems that are carried with it, from simple components to complete systems performing. For address the problem of high complexity has chosen to make a approach that defines new levels of abstraction on the classic logic, such as RTL and functional.

In the approach of the program is part of the course with an introduction

of electrical and logical levels to focus then the greater weight of the subject to structural and functional levels, for introducing the VHDL hardware description language.

2.Profesorado

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Previous 3.Conocimientos required to continue normally the subject

Subjects overcome

Other results learning necessary

• Introduction to Electronics

4. Learning Objectives

Powers assigned to the subject and level of ACQUISITION

Code	**Competition**	**Level**
CG1-CG13	All subjects contribute Curriculum greater or lesser extent to the achievement of the general skills of the graduate profile.	1
CECT9	Capacity for analysis and design of combinational circuits and sequential, synchronous and asynchronous, and use of microprocessors and integrated circuits.	

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CECT10
Knowledge and application of the fundamentals of languages
description of hardware devices
2
LEGEND:
Acquisition Level 1: Basic
Acquisition level 2: Middle
Acquisition Level 3: Advanced

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LEARNING OUTCOMES OF THE COURSE

Code	**Learning result**	**Competition**	**ences associated**	**Level acquisition**	**tion**
RA1	Acquire the fundamental concepts of coding information using different numbering systems	CECT9		2	
RA2	Learn and master Boolean algebra and tools for Simplifying logic functions.	CECT9		2	
RA3	Ability to analyze and design circuits combinational electronic.	CECT9		2	
RA4	Ability to analyze and design circuits sequential electronics.	CECT9		2	
RA5	Be able to apply knowledge acquired on circuits for combinational and sequential design of finite state automata.	CECT9		2	

RA6
Acquire basic knowledge for
analysis and design of electronic circuits
employing digital languages
hardware description.
CECT10
2
RA7
Acquire
LEGEND:
Acquisition Level 1: Knowledge
Acquisition Level 2: Comprehension / Application
Acquisition Level 3: Analysis / Synthesis / Implementation

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5.
System evaluation of the subject
ACHIEVEMENT INDICATORS
Ref
Indicator
Related
do with RA
I1
Know the different numbering systems and
representations of negative numbers in binary.
RA1
I2
Knowing the axioms, properties and basic theorems
Boolean Algebra.
RA2
I3
Being able to simplify a logic function using the
Boolean Algebra.
RA2
I4
Being able to analyze and design an electronic circuit
combinational.
RA3
I5
Being able to analyze and design an electronic circuit
sequentially.
RA4
I6
Being able to analyze and design a state machine
finite.
RA5
I7
Being able to analyze and design a language code
hardware description to simulate an electronic circuit

digital combinational and / or sequential.
RA6
I8
Being able to apply the knowledge acquired in a professionally, interpreting and transmitting data relevant in an autonomous, both in Spanish and English, and making use of new technologies a way that respects the environment.
RA7

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Summative
Brief description of the assessable activities
Time
Place
Weight
the calif.
Resolution and delivery of exercises
The entire course
Classroom
10%
Controls class
The entire course
Classroom
10%
1st Test on Partial Evaluation
(Items 1, 2 and 3 of the contents)
Week 12
Classroom
30%
2nd Test on Partial Evaluation
(Items 4 and 5 of the contents)
Official Date
final exam
Classroom
50%
Total:
100%
Qualification Criteria
Students will be assessed by continuous assessment default. In compliance with the Regulations Assessment of the Technical University of Madrid, Students who wish to be evaluated by a single long final test when you inform the Director of the Department of Electronic Engineering on application to the registry of the School of Telecommunications Engineers before the day November 20, 2012. The presentation of this paper constitute a waiver automatic continuous assessment. The final mark will be obtained through continuous assessment sum of the ratings for the following evaluation activities:

• Resolution and delivery of classroom exercises: mean 10% of the grade end.
• 4-control tests conducted during class time representing A total of 10% of the final grade.
• 2 partial evaluation tests: the first of which represents 30% of the final grade and the second by 50%.

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6. Content and Learning Activities

SPECIFIC CONTENT

Block / Topic / Chapter

Paragraph

Indicators

Related

Topic 1: Coding

Information

1.1 Introduction Digital Electronics
I1
1.2 Abstraction digital (vs. analog. Digital)
I1
1.3 Numbering Systems
I1
1.4 Representation negative numbers
I1
1.5 Boolean algebra. Axioms
I2, I3
1.6 Basic Operators. Truth Table
I2, I3
1.7 Logic gates simple and complex
I2, I3
1.8 Karnaugh Maps
I2, I3
2.1 Introduction to programmable logic devices to hardware description languages (VHDL)
I7

Item 2: Devices

2.2 Structure VHDL code
I7

Programmable Logic (VHDL)

2.3 Basic Syntax
I7

Item 3: Circuits

Combinational

3.1 Multiplexers.
I4, I7
3.2 Interconnection of several MUXes.
I4
3.3 Implementation of functions with MUXes.
I4

3.4 Encoders and Decoders
I4, I7
3.5 Interconnection of multiple coders
I4
3.6 Comparators
I4, I7
3.7 Adder
I4, I7
Nvm 08.03
I4
Item 4: Circuits
Sequential
4.1 Basic bistable element
I5
4.2 Set-Reset Scale.
I5
4.3 Bistable level assets (latch)
I5
4.4 Latch CLK edge assets (flip-flops): type-D,
JK and T-type
I5
4.5 Timing.
I5

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4.6 Records Storage.
I5, I7
4.7 Counters
I5, I7
4.8 Shift registers
I5, I7
Item 5: Automata
5.1 Moore and Mealy machines.
I6
5.2 State Diagram.
I6, I7
5.3 Table of automata transitions.
I6

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7.Breve description of the organizational used and the teaching methods employed
Lectures
Lectures will be used for the display of
content with the help of audiovisual.
CLASSES
PROBLEMS
Be solved in class exercises that serve to implement the

knowledge acquired in the lectures.
PRACTICES
WORK
SELF
Each student will study the contents of the subject
and solve various exercises and problems.
JOBS
GROUP
TUTORING
Be conducted according to current regulations, must go
Students who wish to professor responsible for
group to finalize the date and place of conducting the
tutoring.

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8.Recursos teaching
REFERENCES
Text:
"Digital Design (Principles and Practice)" Third Edition, John
F. Wakerly, Prentice Hall. 2001.
Problems:
Solved Problems in Digital Electronics, Javier Garcia
Zubia, Thomson, 2003.
Consultation:
Digital Fundamentals (9th Edition), Thomas L. Floyd, Prentice
Hall, 2006
Exercises Digital Electronics, Isidoro Padilla, Service
ETSIT Publications, 1988
WEB RESOURCES
Website of the subject: moodle.upm.es
EQUIPMENT
No specific equipment.
Classroom: The designated by the Head of Studies.

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9.Cronograma work of the subject
Week
Classroom Activities
Activities
in
Laboratory
Individual Work
Work
Group
Activities
Evaluation
Others
Week 1

(5 hours)
Section 1.1, 1.2, 1.3 and 1.4
(2 hours)
• Study of the concepts
presented (2 hours)
• Exercises (1 hour)
Week 2
(5 hours)
Sections 1.5, 1.6, 1.7 and 1.8
(2 hours)
• Study of the concepts
presented (2 hours)
• Exercises (1 hour)
Week 3
(5 hours)
Sections 2.1, 2.2
(2 hours)
• Study of the concepts
presented (2 hours)
• Exercises (1 hour)
Week 4
(5 hours)
Section 2.3
(2 hours)
• Study of the concepts
presented (2 hours)
• Exercises (1 hour)
Week 5
(5 hours)
Section 3.1, 3.2 and 3.3
(2 hours)
• Study of the concepts
presented (2 hours)
• Exercises (1 hour)

Week 6
(5 hours)
Sections 3.4 and 3.5
(2 hours)
• Study of the concepts
presented (2 hours)
• Exercises (1 hour)
Week 7
(5 hours)
Apartads 3.6, 3.7 and 3.8
(2 hours)
• Study of the concepts
presented (2 hours)

• Exercises (1 hour)
Week 8
(4 hours)
Examples and resolution
Item 3 Issues
(2 hours)
• Exercises (2 hours)
Week 9
(5 hours)
Sections 4.1, 4.2 and 4.3
(2 hours)
• Study of the concepts
presented (2 hours)
• Exercises (1 hour)
Week 10
(6 hours)
Sections 4.4 and 4.5
(2 hours)
• Study of the concepts
presented (2 hours)
• Exercises (1 hour)
Week 11
(5 hours)
Examples and resolution
Topic 4 Problems
(2 hours)
• Exercises (3 hours)
Week 12
(5 hours)
Sections 4.6, 4.7 and 4.8
(2 hours)
• Study of the concepts
presented (2 hours)
• Exercises (1 hour)
1st partial test
(1 hour)
Week 13
(5 hours)
VHDL circuits
sequential
(2 hours)
• Study of the concepts
presented (2 hours)
• Exercises (1 hour)

Week 14
(6 hours)
Sections 5.1, 5.2 and 5.3

(2 hours)
• Study of the concepts
presented (2 hours)
• Exercises (1 hour)
Delivery exercises
proposed
Week 15
(4 hours)
Examples and resolution
problems with robots
VHDL
(2 hours)
• Exercises (2 hours)
Weeks
16-17-18
(8 hours)
• Study / Exam Preparation Final /
Partial 2nd Test
(6 hours)
Final Exam /
2nd partial test
(2 hours)