DEPARTAMENTO DE INGENIERÍA ELECTRÓNICA

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TESIS DOCTORAL

COMBINED WORD-LENGTH ALLOCATION AND HIGH-LEVEL SYNTHESIS OF DIGITAL SIGNAL PROCESSING CIRCUITS

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ABSTRACT

This work is focused on the synthesis of Digital Signal Processing (DSP) circuits using specific hardware architectures. Due to its complexity, the design process has been subdivided into separate tasks, thus hindering the global optimization of the resulting systems. The author proposes the study of the combination of two major design tasks, Word-Length Allocation (WLA) and High-Level Synthesis (HLS), aiming at the optimization of DSP implementations using modern Field Programmable Gate Array devices (FPGAs).

A multiple word-length approach (MWL) is adopted since it leads to highly optimized implementations. MWL implies the customization of the word-lengths of the signals of an algorithm. This complicates the design, since the number possible assignations between algorithm operations and hardware resources becomes very high. Moreover, this work also considers the use of heterogeneous FPGAs where there are several types of resources: configurable logic-based blocks (LUT-based) and specialized embedded resources. All these issues are addressed in this work and several automatic design techniques are proposed.

The contributions of the Thesis cover the fields of WLA, HLS using FPGAs, and the combined application of WLA and HLS for implementation in FPGAs.

A thorough approach of HLS has been implemented which considers a complete datap-

ath composed of functional units (FUs), registers and multiplexers, as well as heterogeneous FPGA resources (LUT-based and embedded resources). The approach makes use of a resource library that accounts for MWL effects within the set of resources, thus producing highly optimized architectures. This library includes both LUT-based and embedded FPGA resources, which further increase the power of the HLS task. Another important contribution is the introduction of resource usage metrics suitable for heterogeneous-architecture FPGAs.

A novel quantization error estimation based on affine arithmetic (AA) is presented, as well as its practical application to the automatic WLA of LTI and non-linear differentiable DSP systems. The error estimation is based on performing a pre-processing of the algorithm, which produces an expression of the quantization error at the system output. Therefore, the error can be easily computed leading to fast and accurate WLA optimizations.

The analysis of the impact of different optimization techniques during WLA on HLS results is also presented. The variance in the obtained results corroborates the fact that it is worth using a single architecture model during WLA and HLS, and this is only possible by means of combining these tasks.

The actual combination of WLA and HLS has been firstly performed by using a Mixed Integer Linear Programming (MILP) approach. The results prove the validity of the approach and also provide with insights into the combination of the two tasks that are used to generate heuristic synthesis algorithms.

Finally, the global contribution of this thesis is an HLS heuristic algorithm able to perform the combined WLA and HLS of DSP systems for both homogeneous and heterogeneous FPGA architectures. Up to 20% of resource usage reductions are reported, which proves the importance of such a combined approach, providing electronic designers with a design framework that enables highly improved DSP custom hardware implementations.